IN THE CLAIMS:

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- 1. A method for maintaining cache coherency in a system having a first controller and a second controller, comprising:
- 3 selecting a mirror cache line in a second controller to copy data into;
- 4 mirroring the data from a cache line in a first controller to the mirror cache
- 5 line in the second controller; and
- 6 sending a message from the first controller to the second controller
- 7 informing the second controller of cache meta data associated with the mirror
- 8 cache line.
- 1 2. The method of claim 1, wherein the first controller has information
- 2 about the content of the second controller's cache, and the second controller has
- 3 information about the content of the first controller's cache.
- 1 3. The method of claim 1, wherein the cache meta data includes a
- 2 logical unit, a logical block, a dirty bit map, and a cache identifier for the data
- 3 associated with the mirror cache line.
- 1 4. The method of claim 1 further comprising placing the address of
- 2 the mirror cache line into the first controller's hash table.
- 1 5. The method of claim 1 further comprising placing the address of
- 2 the mirror cache line into the first controller's write back queue.

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- 1 6. The method of claim 1 further comprising managing a free list of
 2 mirror locations in the second controller's cache by the first controller, and
 3 managing a free list of mirror locations in the first controller's cache by the
 4 second controller, wherein the first and second controllers can copy data into the
 5 second and first controller's mirror locations, respectively.
- 7. The method of claim 1, further comprising sending a message from the first controller to the second controller, requesting ownership of a cache line owned by the second controller.
 - 8. The method of claim 7, further comprising granting ownership of a cache line owned by the second controller, to the first controller, wherein, subsequent to the first controller receiving data that is to be mirrored to the second controller cache line, transferring data to the second controller's cache line from the first controller.
- 9. The method of claim 8, further comprising sending a message from the first controller to the second controller providing the second controller of cache meta data associated with the mirror cache line.
- 1 10. The method of claim 1, further comprising switching ownership of 2 cache lines between the first controller and the second controller.

- 1 11. The method of claim 1, further comprising, during failback,
- 2 transferring cache lines from a survivor controller that owns a substantial number
- 3 of mirror cache lines, to a replacement controller unit.
- 1 12. The method of claim 1, further comprising, sending a message to a
- 2 controller of a mirror cache line, informing the controller that the associated
- 3 cache line will be flushed and the data associated with the mirror cache line will
- 4 be temporarily invalid.
- 1 13. The method of claim 12, wherein sending the message to the
- 2 controller of the mirror cache line further comprises, informing the controller that
- 3 after the associated cache line is destaged, and the mirror cache line's data is
- 4 consistent with a backing disk and need not be written to the backing disk in the
- 5 event of a failove.
- 1 14. The method of claim 1, further comprising, indicating to the first and
- 2 second controller that a cache line that has been flushed of data, is available for
- 3 reuse.

1	15. <i>A</i>	A controller system for maintaining cache coherency, comprising:
2	a disk a	nrray,
3	a first ¢	ontroller, coupled to the disk array, for selecting a mirror cache line
4	on a second of	ontroller; and
5	an inter	face for mirroring the data from a first controller cache line to the
6	second contro	ller cache line;
7	whereir	a message is sent from the first controller to the second controller
8	informing the	second controller about cache meta data associated with the mirror
9	cache line.	
1	16.	The controller system of claim 15 wherein the first controller has
2	information ab	out the content of the second controller's cache, and the second
3	controller has	information about the content of the first controller's cache.
1	17.	The controller system of claim 15, wherein the cache meta data
2	includes a logi	ical unit, a logical block, a dirty bit map, and a cache identifier
3	associated wit	h the mirror cache line.
1	18.	The controller system of claim 15 further comprising the first
2	controller plac	ing the address of the mirror cache line into the first controller's
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- 1 19. The controller system of claim 15 further comprising the first controller placing the address of the mirror cache line into the first controller's write back queue.
- 1 20. The controller system of claim 15 further comprising the first
 2 controller managing a free list of mirror locations in the second controller's
 3 cache, and the second controller managing a free list of mirror locations in the
 4 first controller's cache, wherein the first and the second controller can copy data
 5 into the second and the first controller mirror locations, respectively.
- 1 21. The controller system of claim 15, further comprising the first
 2 controller sending a message to the second controller, requesting ownership of a
 3 cache line owned by the second controller.
 - 22. The controller system of claim 21, wherein the second controller sends a message granting ownership of a cache line owned by the second controller, to the first controller, wherein, subsequent to the first controller receiving data that is to be mirrored to the second controller cache line, transferring that data to the second controller's cache line from the first controller.

in the event of a failover.

1	23.	The controller system of claim 22, further comprising the first
2	controller se	nding a message from to the second controller informing the second
3	controller of	cache meta data associated with the mirror cache line.
1	24.	The controller system of claim 15, wherein the first and second
2	controllers s	witch ownership of cache lines.
1	25.	The controller system of claim 15, further comprising, during
2	failback, a s	urvivor controller that owns a substantial number of mirror cache
3	lines transfe	rs associated cache lines to a replacement controller unit.
1	26.	The controller system of claim 15, wherein a message is sent to a
2	controller of	a mirror cache line, informing the controller that the associated
3	cache line w	rill be flushed and the data associated with the mirror cache line will
4	be temporar	ily invalid.
1	27.	The controller system of claim 26, wherein the message that is sent
2	to the contro	oller of the mirror cache line further comprises, informing the
3	controller th	at after the associated cache line is destaged, the mirror cache line's
4	data is cons	istent with a backing disk and need not be written to the backing disk

1	28. The controller system of claim 15, further comprising, indicating to		
2	the first and second controller that a cache line that has been flushed of data is		
3	available for reuse.		
1	29. An article of manufacture comprising a program storage medium		
2	readable by a computer, the medium tangibly embodying one or more programs		
3	of instructions executable by the computer to perform a method for maintaining		
4	cache coherency, the method comprising:		
5	selecting a mirror cache line in a second controller to copy data into;		
6	mirroring the data from a cache line in a first controller to the mirror cache		
7	line in the second controller; and		
8	sending a message from the first controller to the second controller		
9	informing the second controller of cache meta data associated with the mirror		
10	cache line.		
1	30. A storage system for maintaining cache coherency, comprising:		
2	means for selecting a mirror cache line in a second controller to copy data		
. 3	into;		
4	means for mirroring the data from a cache line in a first controller to the		
5	mirror cache line in the second controller; and		
6	means for sending a message from the first controller to the second		
7	controller informing the second controller of cache meta data associated with the		
8	mirror cache line.		